CBCS SCHEME

USN | | | | | | | | | | |

20EVE15

First Semester M.Tech. Degree Examination, Feb./Mar. 2022
Digital VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the MOSFET current equation in different regions of operation and plot the current voltage characteristics of an n-channel MOSFET. **(10 Marks)**

b. What is MOSFET Scaling? Explain in brief the types of scaling indicating the effect of scaling on device characteristics. **(10 Marks)**

OR

2 a. Draw a resistance – load inverter circuit and calculate V_{OH} and V_{OL} of the circuit. **(10 Marks)**

b. Consider a resistance load inverter with $V_{DD} = 5V$, $K_n = 20\mu A/V^2$ $V_{TO} = 0.8V$, $R_L = 200k\Omega$ and W/L= 2, find the critical voltage V_{OL}, V_{OH}, V_{IL} and V_{IH}. **(10 Marks)**

Module-2

3 a. Draw the neat diagram of CMOS inverters circuit and explain the circuit operation and calculate the V_{IL}, V_{IH} and V_{th}. **(12 Marks)**

b. Consider a CMOS inverter circuit with the following parameters $V_{DD} = 3.3V$, $V_{TO,n} = 0.6V$, $V_{TO,P} = -0.7V$, $K_n = 200\mu A/V^2$, $K_p = 800\mu A/V^2$. Calculate the noise margins of the circuit. **(08 Marks)**

OR

4 a. Explain CMOS ring Oscillator circuit. What is the expression for frequency in arbitrary odd number (n) of cascade connected inverters. **(10 Marks)**

b. Define propagation delay times T_{PHL} and T_{PLH}. **(05 Marks)**

c. Write a note on Elmore delay. **(05 Marks)**

Module-3

5 a. Discuss in detail about conceptual random access memory array organization with a diagram. **(08 Marks)**

b. Explain about hot electron injection mechanism used for data programming and erasing in flash memory. **(06 Marks)**

c. Design 4×8 NOR based ROM array that can store the following data given in table below, table Q5(c)

Note : R_1, R_2, R_3, R_4 → Address and C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 → memory locations.

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
1	0	0	0	0	1	1	1	0	1	0	0
0	1	0	0	0	1	0	0	0	0	1	0
0	0	1	0	1	0	1	1	0	0	0	0
0	0	0	1	1	1	0	1	0	1	1	1

Table Q5(c) **(06 Marks)**

OR

6 a. Briefly explain about the CMOS SRAM cell with a neat diagram. (10 Marks)
b. What is FRAM? Explain hysteresis characteristics of ferroelectric capacitor. (10 Marks)

Module-4

7 a. What is voltage Bootstrapping? Explain the dynamic Boot strapping circuit. What is the necessity of dummy MOS device for the realization of the Boot strapping capacitor? (10 Marks)
b. Draw a generalized circuit diagram of a domino CMOS logic gate and explain briefly. (10 Marks)

OR

8 a. What is BiCMOS logic circuit? Write the application of it. (06 Marks)
b. Explain the static beheviour of basic BiCMOAS inverter circuits. (10 Marks)
c. Draw the Ebers – M011 equivalent circuit diagram of the npn BJT. (04 Marks)

Module-5

9 a. Discuss in detail about on-chip clock generation and distribution in VLSI chip design. (10 Marks)
b. What are the points to be considered in the design of digital system? (04 Marks)
c. Write a note on ESD protection. (06 Marks)

OR

10 a. Explain the process involved performance modeling with neat diagram. (10 Marks)
b. What is latch up in CMOS? Explain with necessary diagrams and equations. Also discuss guidelines for avoiding latch. (10 Marks)

* * * * *